=[IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

THE TRUSTEES OF PURDUE UNIVERSITY,	§	
Plaintiff	§	
	§	**W-21-CV-00727-ADA-DTG**
-v-	§	
	§	
STMICROELECTRONICS N.V., STMICROELECTRONICS, INC., STMICROELECTRONICS INTERNATIONAL N.V.,	§	
Defendants	§	
	§	

CLAIM CONSTRUCTION ORDER AND MEMORANDUM IN SUPPORT THEREOF

Before the Court are the Parties' claim construction briefs: Defendants STMicroelectronics N.V, STMicroelectronics, Inc., STMicroelectronics International N.V.'s Opening and Reply briefs (ECF Nos. 66 and 74 respectively) and Plaintiff The Trustees of Purdue University's Response and Sur-Reply briefs (ECF Nos. 70 and 76 respectively). The Court provided preliminary constructions for the disputed terms the day before the hearing. The Court held the *Markman* hearing on April 29, 2022. ECF No. 86. During that hearing, the Court informed the Parties of the final constructions for the disputed terms. *Id.* This Order does not alter any of those constructions.

I. DESCRIPTION OF THE ASSERTED PATENTS

Plaintiff asserts U.S. Patent Nos. 7,498,633 and 8,035,112. Both patents are directed towards metal oxide semiconductor field effect transistors (MOSFETS) with silicon carbide (SiC) substrates.

A. The ’633 Patent

The ’633 Patent is entitled “High-Voltage Power Semiconductor Device.” Figure 1 depicts a cross-section of one embodiment of the claimed double-implanted MOSFET (“DMOSFET”). ’633 Patent at 3:50–51 (coloring added by Defendants in Opening at 12), 4: 7–9.

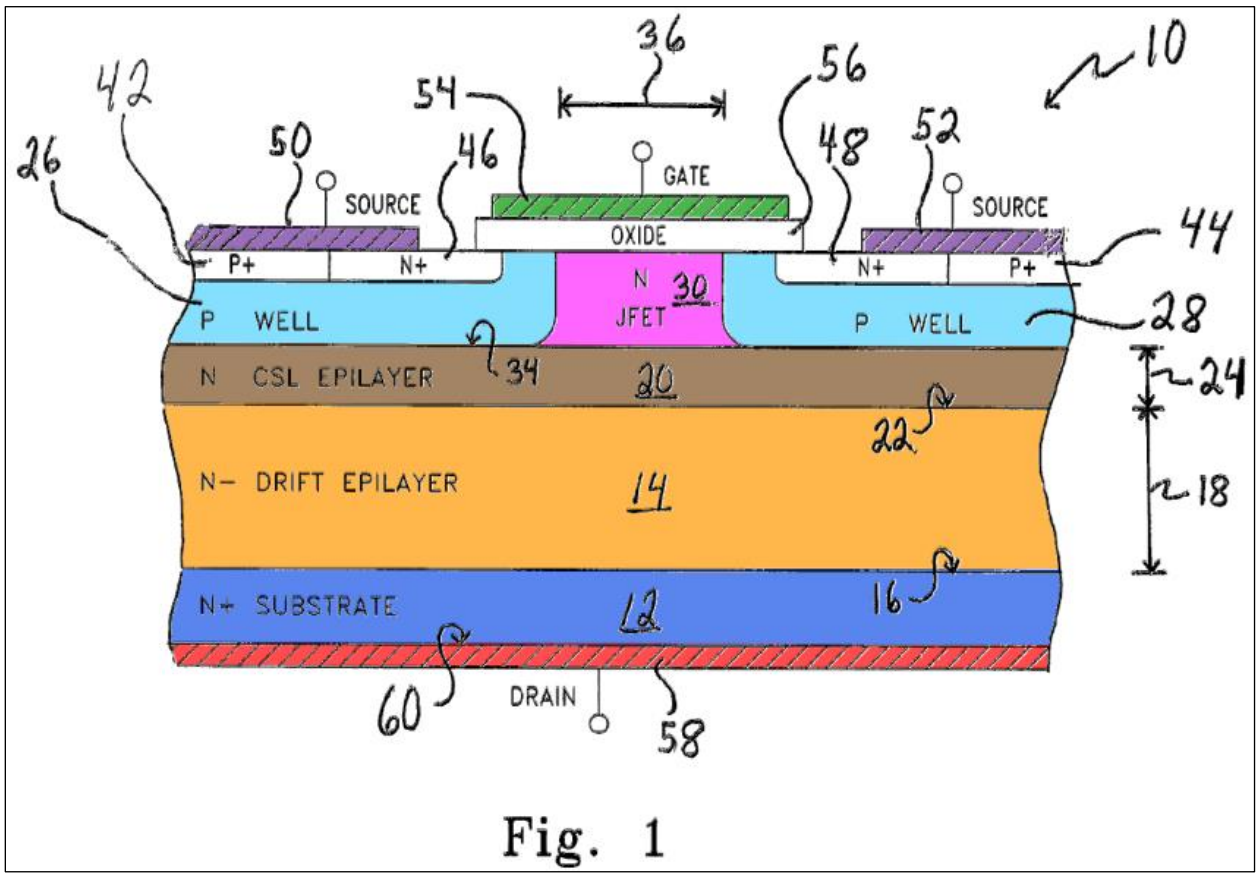


Fig. 1

A DMOSFET acts like a switch, namely, applying a voltage to gate 36 “closes” the switch, which allows current to flow from sources 50 and 52 to drain 58. On the other hand, applying no voltage to gate 36 “opens” the switch, which means that no current flows from sources 50 and 52 to drain 58.

B. The ’112 Patent

The ’112 Patent is entitled “SIC power DMOSFET with self-aligned source contact.” The fabrication of a DMOSFET (or any semiconductor device) involves using different “masks” which are used to “pattern” different features of the semiconductor device. But when different masks as misaligned, then the features that those masks are used to pattern will also be misaligned. Figure 1 depicts when source contact 13 is “perfectly” aligned. ’112 Patent at 3:25–31.

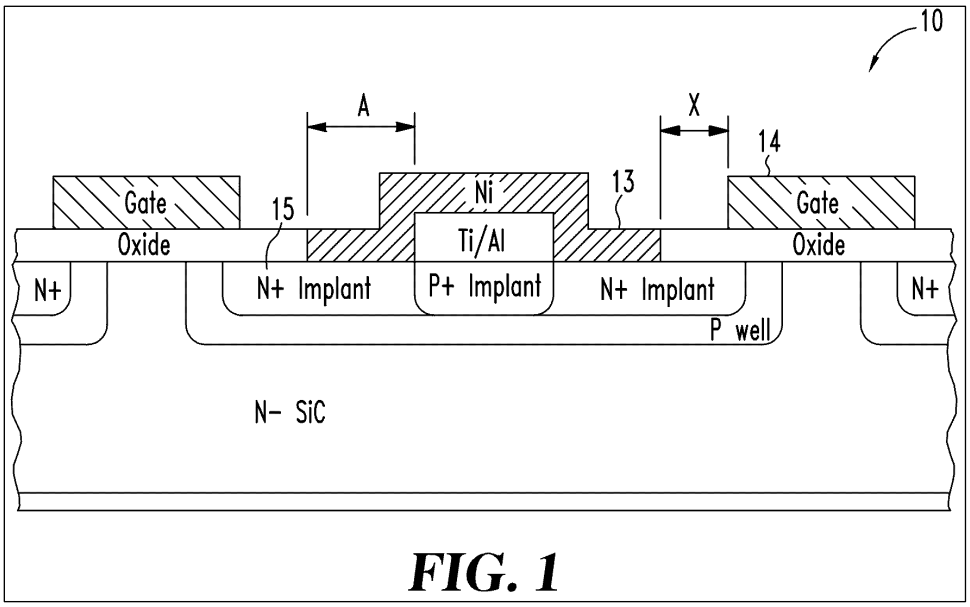


FIG. 1

The specification describes that source contact 13 “must be separated from the edge of the gate 14 by sufficient distance X so that source contact 13 and gate 14 cannot touch even under worst-case misalignment of the source contact mask.” *Id.* at 3:28–31. The specification also describes, on the other hand, that “the actual functional area of the source contact is determined by the overlap A of the source contact metal 13 and the N+ implant 15 that forms the source region in the semiconductor.” *Id.* at 3:31–34.

Figure 2 depicts the “worst-case” mask misalignment where the source contact 13’ is shifted to the right such that overlap B in Figure 2 is “almost zero” and is smaller than overlap A in Figure 1. Figure 2 also depicts that because of this mask misalignment spacing Y in Figure 2 is smaller spacing X in Figure 1.

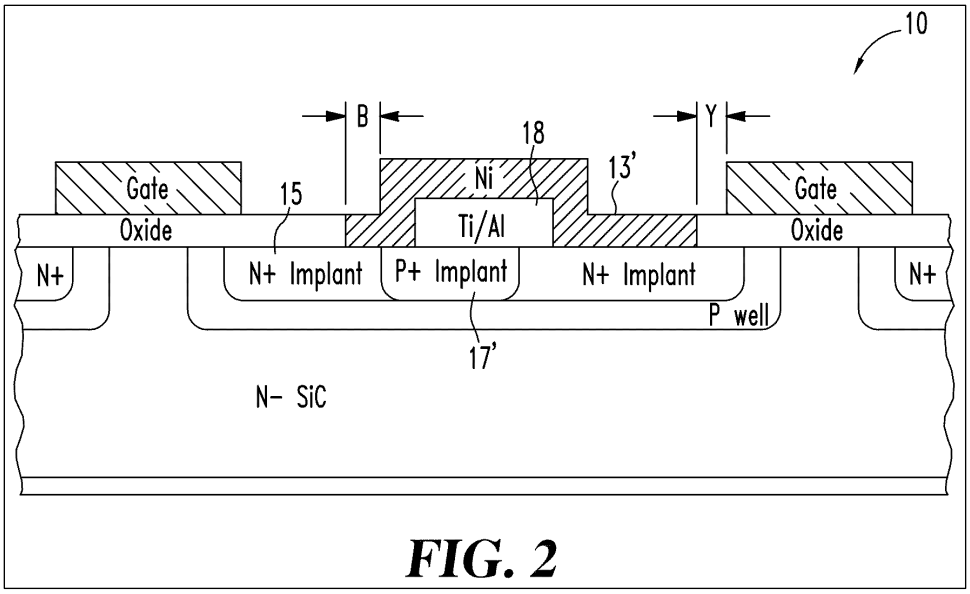


FIG. 2

The specification describes that reducing the functional area of the source contact, *i.e.*, decreasing overlap A to overlap B, increases the source resistance, and that increasing the source resistance degrades the performance of the power DMOSFET. *Id.* at 3:34–38, 3:22–24.

In addition to increasing the source resistance, mask misalignment increases the total area needed for each device as physical designers need to build in sufficient margin so that source contact 13 never touches gate 14. *Id.* at 2:2–6.

The claimed invention purports to solve the problem of mask misalignment by designing the fabrication of DMOSFETs such that the source contact 13 "self-aligns" to gate 14, thereby eliminating the need to use one of the masks that could cause the misalignment. *Id.* at 2:18–26.

Figures 5 to 8 show the cross-sectional view of the DMOSFET during intermediate steps of fabrication. *Id.* at 2:54–57. Figure 5 shows the substrate body 22 below both a 50 nanometer oxidation layer (gate oxidation layer 59) and a 4000 Å thick layer of polysilicon (polysilicon layer 66). *Id.* at 5:47–49, 5:26–32. On top of polysilicon layer 66 is gate mask 62 which is used to pattern to polysilicon layer 66 into gate 38 (depicted in Figure 6). *Id.* at 5:32–34.

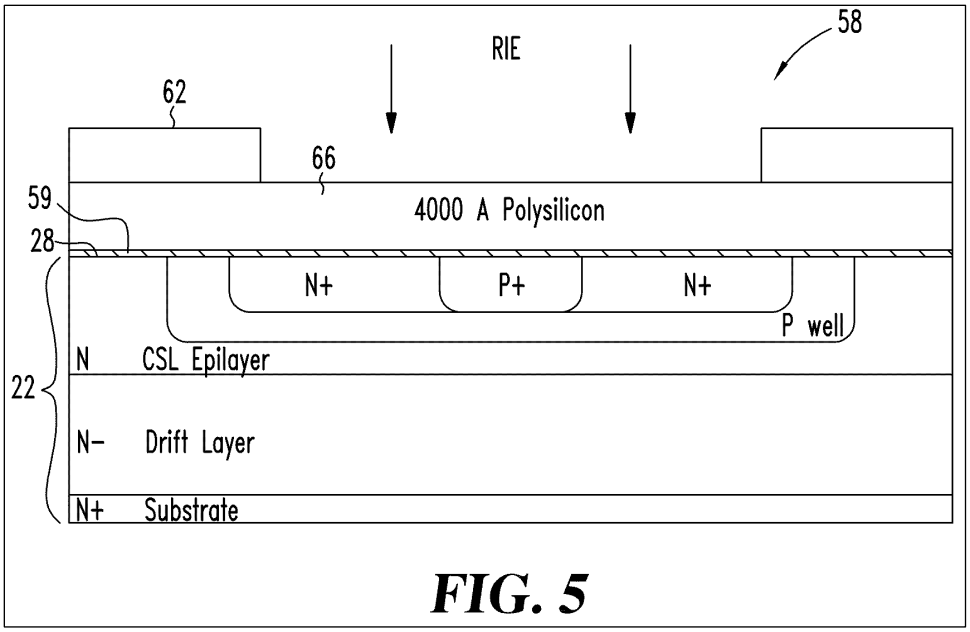


FIG. 5

Figure 5 also depicts the use of a reactive ion etch ("RIE") to etch away the exposed portions of polysilicon layer 66, *i.e.*, not covered by gate mask 62. *Id.*

Figure 6 depicts the cross-sectional view of the DMOSFET after removing exposed portions of polysilicon layer 66 using the RIE and after removing gate mask 62. *Id.* at 5:32–34. Figure 6 depicts that gate 38 are the portions of polysilicon layer 66 that were protected from the RIE by gate mask 62. *Id.* at 5:54–58.

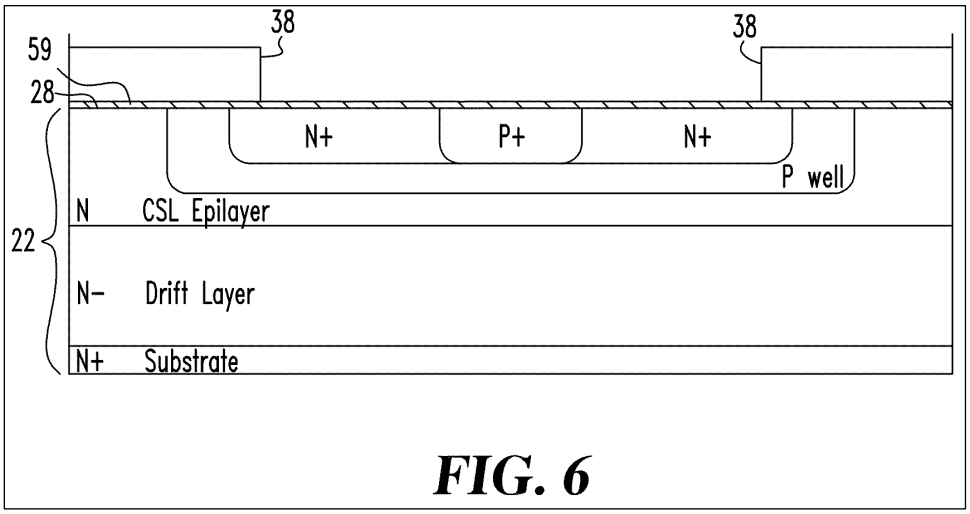


FIG. 6

Figure 7 depicts the cross-sectional view of the DMOSFET after growing oxidation layer 69 on top of and adjacent to gate 38 and oxidation layer 70 on top of gate oxidation layer 59. *Id.* at 6:20–22. The specification describes that oxidation layer 69 is approximately 500 nanometers thick while oxidation layer 70 is only approximately 10 nanometers thick. *Id.* at 6:31–34. The reason that oxidation layer 69 is significantly thicker than oxidation layer 70 is due to the difference in the oxidation rates of polysilicon in gate 38 and the SiC substrate 22, namely, the oxidation growth rate is ten time higher in the former as compared to the latter. *Id.* at 6:27–30.

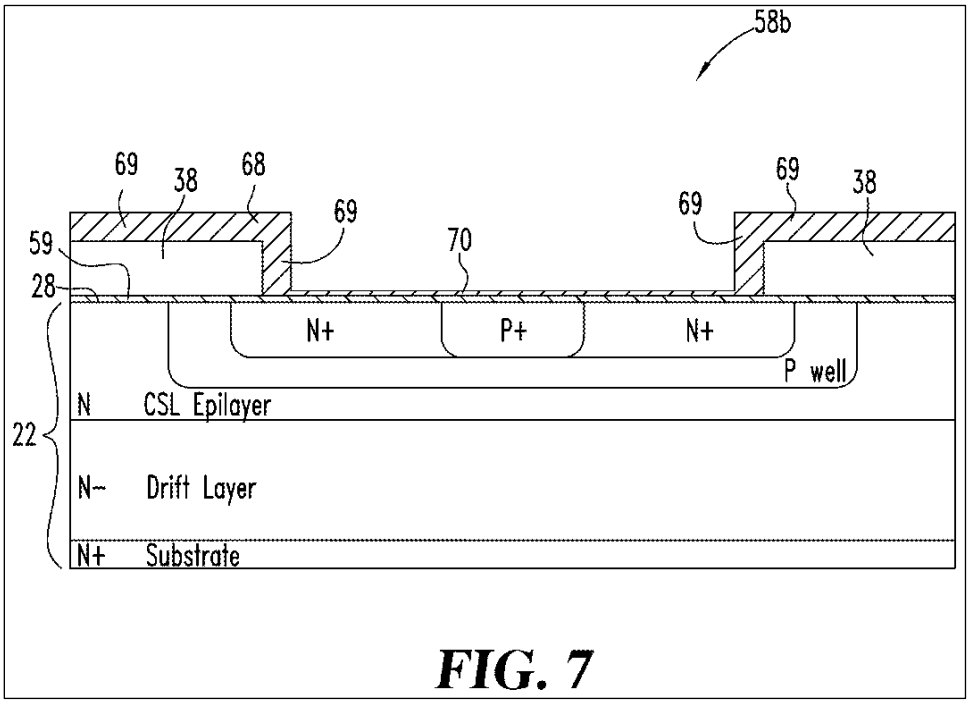


FIG. 7

Therefore, the total thickness of oxidation layer 59 (50 nanometers) and oxidation layer 70 (10 nanometers) is 60 nanometers while the total thickness of oxidation layer 69 is 500 nanometers. *Id.* at 5:47–49, 6:31–34.

The specification describes that the next step is to use a "short" oxide etch to completely remove oxidation layers 59 and 70 and partially remove oxidation layer 69. *Id.* at 6:45–50. The reason that the latter is only partially removed while the former is fully removed is due to the

difference in thicknesses (*i.e.*, 500 nanometers for oxidation layer 69 versus 60 nanometers for oxidation layers 59 and 70). *See id.* Figure 8 depicts the cross-sectional view of the DMOSFET after the "short" oxide etch step.

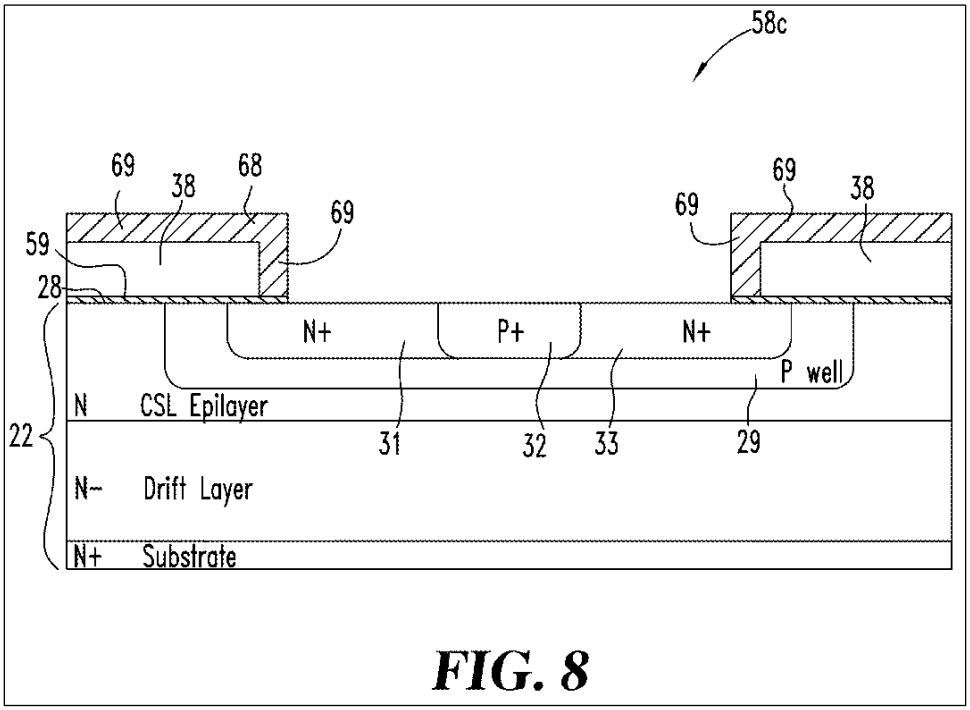


FIG. 8

The specification describes that the next step is to deposit Ti/Al contact metal 43 and Ni contact metal 44 for the ohmic contact to the P well 29. *Id.* 6:52–56. The specification then describes that the following step is to deposit Ni contact metal 45—without using a mask—for the ohmic contact to N+ source implants 31 and 32. *Id.* at 6:57–62.

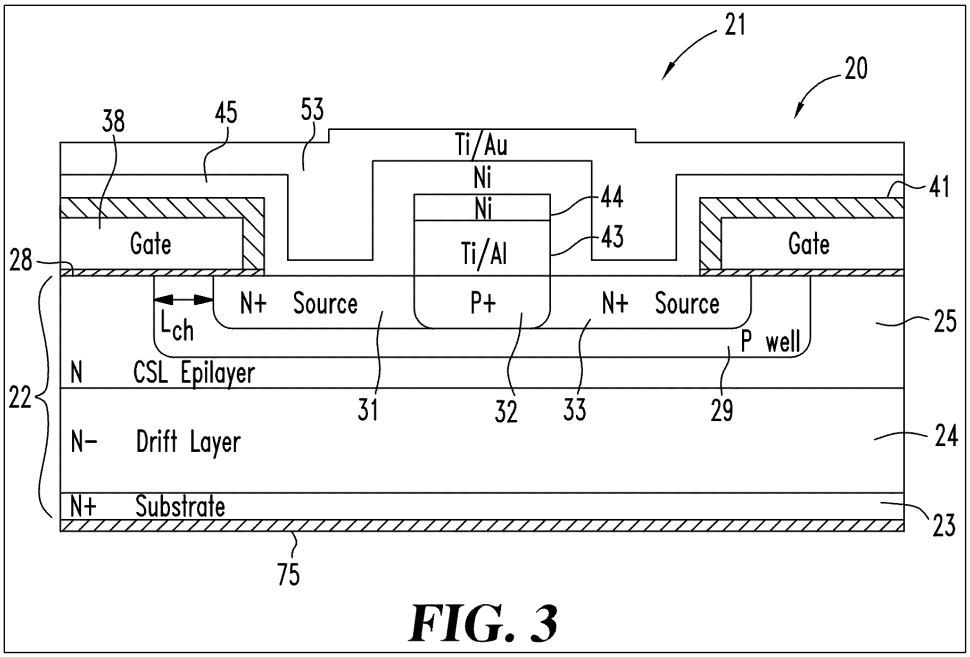


FIG. 3

Because Ni contact metal 45 is deposited without using a mask, Ni contact metal is deposited over the entire top surface of semiconductor device 58c. *Id.* But because thick oxide layer 41 separates—both physically and electrically—gate 38 from Ni contact metal 45, this does not result in an electrical short-circuit between gate 38 and Ni contact metal 45. *Id.* at 6:62–63. In other words, the presence of thick oxide layer 41 eliminates the need to use a mask—thus eliminating the potential for mask misalignment—to deposit Ni contact metal 45, while also preventing an electrical short-circuit between gate 38 and Ni contact metal 45. *Id.* at 6:63–66. The specification describes that benefits of the claimed invention are:

> the area of the functional source contact is not determined by the alignment of any masking levels and is not subject to random misalignments during processing. Instead, it is totally determined by the spacing between adjacent polysilicon gates and is, in fact, self-aligned to the gate level, being separated by the thickness of the oxide layer covering the gate. This eliminates the alignment tolerance (X or Y in FIGS. 1 and 2), thus reducing the cell area and the specific on-resistance.

Id. at 6:63–7:4.

II. LEGAL STANDARD

A. General principles

The general rule is that claim terms are generally given their plain-and-ordinary meaning. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*); *Azure Networks, LLC v. CSR PLC*, 771 F.3d 1336, 1347 (Fed. Cir. 2014), *vacated on other grounds*, 575 U.S. 959, 959 (2015) ("There is a heavy presumption that claim terms carry their accustomed meaning in the relevant community at the relevant time.") (internal quotation omitted). The plain-and-ordinary meaning of a term is the "meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Phillips*, 415 F.3d at 1313.

The "only two exceptions to [the] general rule" that claim terms are construed according to their plain-and-ordinary meaning are when the patentee (1) acts as his/her own lexicographer or (2) disavows the full scope of the claim term either in the specification or during prosecution. *Thorner v. Sony Computer Ent. Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). The Federal Circuit has counseled that "[t]he standards for finding lexicography and disavowal are exacting." *Hill-Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1371 (Fed. Cir. 2014). To act as his/her own lexicographer, the patentee must "clearly set forth a definition of the disputed claim term" and "'clearly express an intent' to [define] the term." *Thorner*, 669 F.3d at 1365.

"Like the specification, the prosecution history provides evidence of how the PTO and the inventor understood the patent." *Phillips*, 415 F.3d at 1317. "[D]istinguishing the claimed invention over the prior art, an applicant is indicating what a claim does not cover." *Spectrum Int'l, Inc. v. Sterilite Corp.*, 164 F.3d 1372, 1379 (Fed. Cir. 1998). The doctrine of prosecution disclaimer precludes a patentee from recapturing a specific meaning that was previously disclaimed during prosecution. *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1323 (Fed. Cir. 2003). "[F]or prosecution disclaimer to attach, our precedent requires that the alleged disavowing

actions or statements made during prosecution be both clear and unmistakable." *Id.* at 1325–26. Accordingly, when "an applicant's statements are amenable to multiple reasonable interpretations, they cannot be deemed clear and unmistakable." *3M Innovative Props. Co. v. Tredegar Corp.*, 725 F.3d 1315, 1326 (Fed. Cir. 2013).

A construction of "plain and ordinary meaning" may be inadequate when a term has more than one "ordinary" meaning or when reliance on a term's "ordinary" meaning does not resolve the parties' dispute. *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1361 (Fed. Cir. 2008). In that case, the Court must describe what the plain-and-ordinary meaning is. *Id.*

"Although the specification may aid the court in interpreting the meaning of disputed claim language . . ., particular embodiments and examples appearing in the specification will not generally be read into the claims." *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1571 (Fed. Cir. 1988). "[I]t is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004).

An applicant's statements during the PCT prosecution may also indicate the scope of the invention. *See Caterpillar Tractor Co. v. Berco*, 714 F.2d 1110, 1116 (Fed. Cir. 1983) (stating that when instructions to foreign counsel or representations to foreign patent offices made by an applicant during prosecution of a corresponding foreign application provide "relevant evidence" with respect to claim interpretation, such information "must be considered."); *see also Gillette Co. v. Energizer Holdings, Inc.*, 405 F.3d 1367, 1374 (Fed. Cir. 2005) (finding that the applicant's own statements made before the European Patent office support the court's holding).

Although extrinsic evidence can be useful, it is "less significant than the intrinsic record in determining 'the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc. v. United States Surgical Corp.*, 388 F.3d 858, 862 (Fed. Cir. 2004)). Technical dictionaries may be helpful, but they may also provide definitions that are too broad or not indicative of how the term is used in the patent. *Id.* at 1318. Expert testimony may also be helpful, but an expert's conclusory or unsupported assertions as to the meaning of a term are not. *Id.*

B. Whether the Preamble is Limiting

Courts presume that the preamble does not limit the claims. *Am. Med. Sys., Inc. v. Biolitec, Inc.*, 618 F.3d 1354, 1358 (Fed. Cir. 2010). But "[i]n general, a preamble limits the invention if it recites essential structure or steps, or if it is 'necessary to give life, meaning, and vitality' to the claim." *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002) (quoting *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 (Fed. Cir. 1999)). "Conversely, a preamble is not limiting 'where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention.'" *Catalina*, 289 F.3d at 808 (quoting *Rowe v. Dror*, 112 F.3d 473, 478 (Fed. Cir. 1997)). The Federal Circuit has provided some "guideposts" regarding whether the preamble is limiting: (1) preamble provides antecedent basis, (2) preamble is essential to understand limitations or terms in the claim body, (3) preamble recites "additional structure or steps underscored as important by the specification," and (4) "clear reliance on the preamble during prosecution to distinguish the claimed invention from the prior art." *Id.*

C. Indefiniteness

"[I]ndefiniteness is a question of law and in effect part of claim construction." *ePlus, Inc. v. Lawson Software, Inc.*, 700 F.3d 509, 517 (Fed. Cir. 2012). Patent claims must particularly point out and distinctly claim the subject matter regarded as the invention. 35 U.S.C. § 112, ¶ 2. A claim, when viewed in light of the intrinsic evidence, must "inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 910 (2014). If it does not, the claim fails § 112, ¶ 2 and is therefore invalid as indefinite. *Id.* at 901. Whether a claim is indefinite is determined from the perspective of one of ordinary skill in the art as of the time the application was filed. *Id.* at 911.

III. LEGAL ANALYSIS

A. Term #1: "a second, thicker oxide layer" / "a gate oxide layer"

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"a second, thicker oxide layer" / "a gate oxide layer" U.S. Patent No. 8,035,112, Cls. 1, 6	"layer of oxide that is on the tops and sides of each gate and that is thicker than the layer of oxide below each gate"	"an oxidation layer formed, created, or grown by reacting the gate, thicker than the first oxide layer"

The Parties' Positions:

The parties dispute whether the oxide layer can only be grown (Defendants' position) or if may be grown or deposited (Plaintiff's position). There are at least two ways of adding an oxide to a semiconductor: deposition (where the oxide falls like snowflakes onto the substrate) or growth (where oxygen reacts with exposed silicon). Defendants contend that the patentee limited their invention to the second method. *See, e.g.*, Opening at 9. Plaintiff contends that the patentee did not so limit their invention. *See, e.g.*, Response at 3.

Defendants contend that the specification describes the scope of the invention as being limited to growth only, *i.e.*, excludes deposition. Opening at 9. In particular, Defendants point to the following passage in the specification:

> ***Alternative embodiments are contemplated*** wherein the secondary steps (and even certain of the primary steps) can be performed in ways other than recited, with materials, solutions and concentrations other than recited, and for times and under temperatures and conditions other than recited, ***so long as the gate and substrate source (or other ohmic contact materials) react to form, create or grow an insulation layer (such as SiO2)*** sufficiently faster, larger and/or with more insulating capacity at the gate surface than at the substrate surface and that will therefore be uniformly removable at a rate which will remove all such formed, created or grown layer substantially or entirely completely from the substrate surface and leave a sufficiently insulative layer around the gate.

Id. at 10 (citing '112 Patent at 7:20–33) (emphasis in Defendants' brief). Defendants contend that growing the oxide layer (as compared to depositing the oxide layer) is how the patent achieves "self-aligned source contacts." *Id.* (citing '112 Patent at Title, 1:21–23, 2:24–26, 3:57–59, 6:63–7:2). Defendants contend that statements directed to the "present invention" limit the scope of the term. *Id.* at 10–11 (citing *Regents of the Univ. of Minn. v. AGA Med. Corp.*, 717 F.3d 929, 936 (Fed. Cir. 2013)). Defendants further contend that the "whole point of the purported invention" is that only a very thin oxide layer forms on the SiC substrate while a thick oxide layer forms on the polysilicon gate. *Id.* at 11.

Defendants contend that Plaintiff's proposed construction "improperly broaden the claims' scope to cover the very oxide deposition and masking process the patent purports to obviate." *Id.*

In its response, Plaintiff contends that Defendants' proposed construction is directed towards a method, but the claim is an apparatus claim. Response at 3. Plaintiff contends its proposed construction is consistent with the claim language and the specification, and provides clarity as to the structure of the claim product itself, rather than the process by which it is made. *Id.* at 4. Plaintiff next contends that Defendants "admit[]" that Plaintiff's proposed construction is

"accurate." *Id.* at 5 (quoting Opening at 9 ("the disputed terms—'a second, thicker oxide layer' (claim 1) and 'a gate oxide layer' (claim 6)—refer to the layer of oxide that is located over the top and sides of the gates.")). Plaintiff further contends that the prosecution history supports its proposed construction. *Id.* More specifically, Plaintiff contends that the PTO issued a restriction requirement which required that Applicant needed to choose between product and method claims. *Id.* at 5–6. Plaintiff contends that because Applicant chose the product claims, Defendants' proposed construction improperly attempts to "resurrect" the method claims. *Id.* at 6.

Plaintiff contends that Defendants' proposed construction is also flawed because "it attempts to restrict the claims to a single method of making one particular embodiment, even though the specification makes clear that the fabrication of the claimed products can be accomplished in various ways," and nothing else in the specification or claims limit how the claimed invention can be made. *Id.* (citing '112 Patent at 5:34–46, 3:2–89).

In their reply, Defendants first contend that their proposed construction does not improperly add a method step to an apparatus claim, but rather describes that "formed, created, or grown by reacting the gate" is "an essential characteristic of the oxidation layer based on its formation (like "dry-aged" steak, "cold-brew" coffee, or "forged" steel)." Reply at 1. Defendants contend Applicant made an explicit disavowal of claim scope by stating that alternative embodiments are contemplated "so long as the gate and substrate source (or other ohmic contact materials) react to form, create or grow an insulation layer (such as SiO_2) sufficiently faster, larger and/or with more insulating capacity at the gate surface than at the substrate surface." *Id.* at 1–2 (quoting '112 Patent at 7:20–33); *see also id.* at 3. Defendants contend that the specification repeatedly identifies the "present invention" as a DMOSFET with self-aligned source contacts, "which are enabled by growing the oxide layer around the gate (as opposed to the disfavored

approach of using a deposited oxide layer, then creating an opening using a mask)." *Id.* at 2. Defendants contend that the provisional application similarly describes the necessity of using grown oxide. *Id.* (citing '112 Patent at 1:7–9 (incorporating provisional application)).

Defendants contend that a textbook (Baliga) incorporated by reference further demonstrates their construction is correct. *Id.* In particular, Defendants contend that the Baliga textbook describes deposited oxides having alignment problems and that the '112 Patent attempts to solve that problem by using grown oxides. *Id.* at 2. Defendants contend that this description and the alternative of growing oxides in the patent provide a clear contrast between the two. *Id.* at 2–3.

With respect to Plaintiff's argument that their proposed construction adds a method step to an apparatus claim, Defendants contend that a process "can be treated as part of a product claim if the patentee has made clear that the process steps are an essential part of the claimed invention." *Id.* at 4 (quoting *Andersen Corp. v. Fiber Composites, LLC*, 474 F.3d 1361, 1375 (Fed. Cir. 2007)).

With respect to Plaintiff's argument that Applicant elected to pursue apparatus claims during prosecution, Defendants essentially argue that Plaintiff's citations of the prosecution history were taken out of context. *Id.* Defendants contend that neither the Examiner or Applicant claimed the oxide layer of the product claims could be formed by any other method than growth. *Id.* Rather, Defendants contend that the prosecution history supports its proposed construction, namely:

> **[A]pplicant's invention provides for** a SiC substrate and polysilicon gates because **growth of the oxidation layer** on the polysilicon gates occurs considerably faster than on the SiC substrate, which creates a much thinner combined oxide layer between adjacent gates (as shown in Fig. 7 of the application) than is simultaneously formed on the tops and sides of such gates. Thus, after a short oxide etch is applied, long enough to completely remove the thin, combined oxide layer over the substrate surface (and between the gates), there is still left a very thick insulating oxide layer on the tops and sides of gates. **This is more than**

> **an obvious design choice and is nowhere disclosed, taught or suggested by Miura**.

Id. at 5 (quoting Ex. E, May 23, 2011 (Response to Office Action at 12)) (emphasis added by Defendants).

In its sur-reply, Plaintiff contends that Defendants' proposed construction does not provide any structure, but rather is "based on formation," which is an improper method step. Sur-Reply at 1. Plaintiff contends that unlike "dry-aged steak," the specification recites that the fabrication of the claimed product "can be accomplished in a variety of ways well known in the art." *Id.* at 1–2 (quoting '112 Patent at 5:36–37; citing '112 Patent at 5:34-46). Plaintiff contends that in light of the disclosures in the specification, there is no "clear and unmistakable" disavowal of claim scope. *Id.* at 2 (citing *Continental Circuits LLC v. Intel Corp.*, No. 2018-1076 (Fed. Cir. Feb. 8, 2019)). According to Plaintiff, in *Continental*, (1) the specification repeatedly distinguished the process covered by the patent from the prior art and its use of a "single desmear process" and (2) characterized the "present invention" as using a repeated desmear process. *Id*. By contrast, Plaintiff contends that Defendants only point to a single "so long as" in the specification. *Id*. Plaintiff contends that this is not a clear and unmistakable disclaimer. *Id*.

With respect to the Baliga textbook, Plaintiff contends that the textbook is "irrelevant" because the context in which the patent describes it is in regards to different types of MOSFETs and not making oxide layers. *Id.* at 3.

The Court's Analysis:

After reviewing the parties' arguments and considering the applicable law, the Court agrees with Plaintiff that there is no disclaimer and that this term should be construed according to its plain-and-ordinary meaning.

As described above, the "heavy presumption" is that terms should be construed according to their plain-and-ordinary meaning. *Azure Networks*, 771 F.3d at 1347. Defendants allege the patentee made a disclaimer, which is one of the two exceptions to the general rule that a term should be construed as having its plain-and-ordinary meaning. *Thorner*, 669 F.3d at 1365. The standard for finding disclaimer is "exacting." *Hill-Rom Servs.*, 755 F.3d at 1371. A disclaimer must be both "clear and unmistakable." *Omega Eng'g*, 334 F.3d at 1325–26. The Court does not find that the Defendants have met the exacting standards to show that there was a clear and unmistakable disclaimer.

Defendant's basis for disclaimer centers around the following passage:

> Alternative embodiments are contemplated wherein the secondary steps (and even certain of the primary steps) can be performed in ways other than recited, with materials, solutions and concentrations other than recited, and for times and under temperatures and conditions other than recited, so long as the gate and substrate source (or other ohmic contact materials) react to form, create or grow an insulation layer (such as SiO2) sufficiently faster, larger and/or with more insulating capacity at the gate surface than at the substrate surface and that will therefore be uniformly removable at a rate which will remove all such formed, created or grown layer substantially or entirely completely from the substrate surface and leave a sufficiently insulative layer around the gate.

'112 Patent at 7:20–33. The Court concludes that this passage does not meet the "exacting" required for disclaimer for at least the following reasons. ***First***, reading this passage in context indicates that the "alternative embodiments" simply vary the primary and secondary steps listed in Appendix II. More specifically, the paragraph in which the above passage appears begins with the following sentence: "The primary processing steps described herein are accompanied by numerous secondary steps (such as 'RCA clean (right before gate oxidation)' and 'DI rinse: 6 times'), all of which are listed recited in Appendix II. Alternative embodiments are contemplated…" *Id.* at 6:17–21. A POSITA reading the above passage in context with the first sentence of the paragraph would understand that the alternative embodiments in above passage relate to variations of the

secondary steps (and even some of the primary steps) listed in Appendix II. By contrast, there is nothing in the above passage from which a POSITA would understand that the above passage refers to all undisclosed embodiments, as Defendants essentially contends. Rather, the "alternative embodiments" are simply minor variations of the exemplary embodiment described in Appendix II. Therefore, the Court concludes that the disclosure in the above passage does not meet the "exacting" standard necessary to show that there is a "clear and unmistakable" disclaimer.

Second, with respect to Defendants' argument that grown oxides are required to implement the claimed invention, the Court disagrees. Rather, based on disclosure in the specification, all that is needed to achieve the self-alignment is to have two oxide layers, where the second layer is much thicker than the first.

Third, with respect to Defendants' prosecution history argument, Applicant's prosecution statements merely describe that the claimed invention differed from the Miura prior art in that there are different oxide thicknesses over the polysilicon gate and the SiC substrate, which meant that an oxide etch would completely remove the oxide over the latter while not completely removing the oxide in the former. While these prosecution statements describe that the oxide growth on polysilicon gates is "considerably faster" than on the SiC substrate, none of the prosecution statements meet the "exacting" standard of a "clear and unmistakable" disclaimer.

Fourth, with respect to the Baliga textbook, the Court agrees with Plaintiff because the '112 Patent incorporated the Baliga textbook for its disclosure of different types of MOSFETs and not for its disclosure of depositing or growing oxide layers. Furthermore, the Court finds that Defendants' argument requires some inferences, which prevents it from meeting the "clear and unmistakable" requirement necessary for a disclaimer.

Fifth, after reviewing the specification, the Court does not agree with Defendants' that the specification's description of the "present invention" limits the scope of this claim term to grown oxides. Most of the time, the specification uses the phrase "the present invention" in a general, non-descriptive way. *See, e.g.*, *id.* at 2:38-41 ("These and other aspects and advantages of the present invention will become more apparent upon reading the following detailed description of preferred embodiments in conjunction with the accompanying drawings."), 2:49–50 ("FIG. 3 is a side, cross-sectional view of one cell region 20 of a DMOSFET 21 in accordance with the present invention."), 4:60–63 ("Referring to FIG. 3, there is shown one cell region 20 of a double-diffused, power metal-oxide-semiconductor field effect transistor (DMOSFET) 21 in accordance with the present invention."). In two instances, the specification describes that the present invention produces self-aligned source contacts. *Id.* at 2:24–26 ("The present invention provides high voltage power MOSFETs, with self-aligned source contacts and a method for making the same."), 3:52–58 ("Both these problems—increased contact resistance at reduced area overlap B from mask misalignment and increased cell width to ensure adequate spacing Y—are eliminated in the present invention by negating the opportunity for misalignment of source contact metal and gate."). But neither of these passages constitutes a "clear and unmistakable" disclaimer. More specifically, as described above, the specification achieves self-alignment by having two oxide layers, where the second layer is much thicker than the first. These passages do not disclose that growing oxides is the only way to achieve a thicker second oxide layer.

Sixth, because Applicant chose the product claims in response to a restriction requirement, limiting how the claimed invention can be fabricated contravenes Applicant's election during prosecution.

Therefore, for the reasons described above, the Court concludes that Defendants have not met the "exacting" standard necessary to show that the patentee made a "clear and unmistakable" disclaimer. As such, the Court's final construction for "a second, thicker oxide layer" and "a gate oxide layer" is plain-and-ordinary meaning.

B. Term #2: "double-implanted metal-oxide semiconductor field effect transistor"

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"double-implanted metal-oxide semiconductor field effect transistor" U.S. Patent No. 7,498,633, Cl. 9	The preamble is not limiting. In the alternative only, "double-implanted" is not limiting.	The preamble **is** limiting.

The Parties' Positions:

The parties primarily dispute whether "double-implanted" is limiting, but more generally, the parties dispute whether the both "double-implanted" and "MOSFET" are limiting. The parties agree that the only basis that the preamble might be limiting is it "gives life, meaning, and vitality and meaning" or recites essential structure. Opening at 13; Response at 8.

Defendants first contend that without the preamble, Claim 9 is structurally incomplete. Opening at 14. In particular, Defendants contend that the claim body is missing certain components of a MOSFET (gate, insulator, and drain), which the preamble provides. *Id.*

Defendants next contend that preamble "contextualizes the possible arrangements and cooperation of those elements. *Id.* More specifically, Defendants contend that "MOSFET" in the preamble "provides necessary context regarding how components must be arranged so as to result in a FET, rather than another device." *Id.* at 14–15.

Defendants then contend that the preamble "fundamentally informs what type of semiconductor device is being claimed: a double-implanted MOSFET, as opposed to another type of transistor." *Id.* at 15. In particular, Defendants contend that because the specification describes a number of embodiments, by specifying "double-implanted MOSFET" in the preamble, a POSITA would understand that the scope of Claim 9 was different than the scope of Claim 1. *Id.*

In its response, Plaintiff contends that "the preamble is not 'essential' to understanding the claim body based on the entirety of the '633 Patent." Response at 8. Plaintiff further contends that the '633 Patent "relates generally to semiconductor devices, and more particularly to semiconductor devices for high-voltage power applications." *Id.* (quoting '633 patent at 1:12–13; Abstract).

Plaintiff contends that the specification describes various MOSFETs including DMOSFETs, and a POSITA would look to the specification. *Id.* at 8–9 (citing 1:40–2:15, 2:16–3:40, 4:4-12, Fig. 1). Plaintiff further contends that a POSITA would understand that the claim language discloses DMOSFETs. *Id.* at 9 (citing '633 Patent, Cl. 9, Lims. [e], [h]).

In their reply, Defendants contend that Plaintiff "does not dispute that the claim body is missing essential MOSFET elements, including a gate, gate insulator, and drain." Reply at 5. Defendants contend that without the preamble, the claim could read on other types of transistors. *Id.*

With respect to Plaintiff's argument that the specification describes various MOSFETs including DMOSFETs, and a POSITA would look to the specification to see which MOSFETS might be claimed, Defendants contend that this point confirms Defendant's argument. *Id.* at 6. More specifically, Defendants contend that because Plaintiff contends that a POSITA would look

to the specification, Plaintiff implicitly concedes that the claim body does not have the DMOSFET language. *Id.*

In its sur-reply, Plaintiff contends that the preamble is "not limiting because it merely provides context for and a descriptive name to the set of limitations, such as silicon-carbide substrate and the JFET-region." Sur-Reply at 4. Plaintiff contends that "a POSITA would understand that Claim 9 is directed to a double-implanted semiconductor device based on the claim elements, without the preamble." *Id.* More specifically, Plaintiff contends that because Claim 9 recites a first and second base contact region and that "the second implant is the plurality of the base contact regions defined in the first implant which is the source region," the claim language itself describes what is "double implanted." *Id.* Plaintiff contends that the specification contemplates multiple types of MOSFETs so Claim 9 should not be limited to a specific one. Sur-*Id.* at 4–5.

With respect to the parties' dispute whether a POSITA would need to consult the specification, Plaintiff contends that Defendants are trying to have it both ways, namely, it wants to look at the claims in light of the specification, but also wants to look at the claim in isolation. *Id.*

The Court's Analysis:

After reviewing the parties' arguments and considering the applicable law, the Court agrees with Defendants that the entire preamble is limiting. As a preliminary note, the Court notes that the presumption is that the preamble is not limiting. Claim 9 provides (annotations added):

> 9. A double-implanted metal-oxide semiconductor field-effect transistor comprising:
> [a] a silicon-carbide substrate;
> [b] a drift semiconductor layer formed on a front side of the semiconductor substrate;
> [c] a first source region;

[d] a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis;
[e] a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode;
[f] a second source region;
[g] a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis;
[h] a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode; and
[i] a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

With respect to whether "MOSFET" in the preamble should be limiting, the Court concludes that this part of the preamble is limiting for the reasons that follow. ***First***, the Court agrees with Defendants that because the claim body only recites some elements of the MOSFET, the preamble provides essential structure. *Catalina.*, 289 F.3d at 808. In particular, the claim body describes that the claimed invention comprises a "source region," which is one part of field-effect transistor (FET). *See, e.g.*, '633 Patent, Claim 9, Lim. [c]. The claim body also describes that the claimed invention uses a silicon-carbide substrate, which a POSITA would understand to correspond to the "S" (semiconductor) in MOSFET. *Id.*, Claim 9, Lim. [a]. But the claim body does not recite the remaining elements of the MOSFET, *e.g.*, gate, gate insulator, and drain. Without these additional elements, the semiconductor may not be a MOSFET, but rather could be another type of semiconductor device. As such, the claim body does not provide a "structurally complete invention such that deletion of the preamble phrase does not affect the structure…of the claimed invention." *Catalina*, 289 F.3d at 809.

Plaintiff does not dispute that the claim body does not recite these additional elements, but rather only asserts that the specification describes these additional elements. Response at 8–9. The Court disagrees with Plaintiff that the preamble is not limiting if the specification describes

these additional elements because whether the specification describes essential structure or not is not the law; rather, a preamble is limiting if it "gives life, meaning, and vitality and meaning" or recites essential structure. *Catalina*, 289 F.3d at 808. Here, as described immediately above, the preamble recites essential structure. Furthermore, under Plaintiff's logic, a preamble would rarely be limiting because most specifications disclose the essential structure provided by the preamble.

Second, Plaintiff implicitly concedes that "MOSFET" is limiting through its alternate construction, which recites that only "double-implanted" in the preamble should not be limiting.

With respect to whether "double-implanted" in the preamble should be limiting, the Court concludes that this part of the preamble is limiting for the reasons that follow. ***First***, the parties agree—or at least Plaintiff does not appear to dispute—that the claim body does not recite a complete invention. A double-implanted MOSFET is a specific type of MOSFET and one that may have different electrical characteristics as compared to a MOSFET that does not use double-implantation. Accordingly, "double-implanted" recites essential structure.

Second, the Court disagrees with Plaintiff that the claim body recites "double-implanted." As described above, Plaintiff contends that a POSITA would understand that the claim language—specifically limitations [e] and [h]—discloses a DMOSFET. Response at 9–10. But these two limitations only require that the claim invention has "base contact regions," and not necessarily that the base contact regions are formed via ion implantation, let alone that there is a double-implantation. Accordingly, "double-implanted" recites essential structure.

Third, for the same reasons there were described above with respect to "MOSFET," the Court disagrees with Plaintiff that because the specification discloses double-implanted MOSFETs, "double-implanted" in the preamble should not be limiting.

Therefore, for the reasons described above, the Court concludes that Defendants have overcome the presumption that the preamble is not limiting. As such, the Court's final construction is that the entire preamble for Claim 9 of the '633 Patent is limiting.

C. Term #3: "less than about three micrometers"

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"less than about three micrometers" U.S. Patent No. 7,498,633, Cl. 9	Plain and ordinary meaning, no construction necessary.	Indefinite

The Parties' Positions:

Defendants contend that this term is indefinite because a POSITA would not be able to determine either the upper boundary or lower boundary. Opening at 16.

With respect to the lower boundary, Defendants contend that "there is no basis for reasonably determining the lower end of the 'less than about three micrometers' range of JFET widths," as it would include "any dimension down to zero width," and the'633 Patent does not "disclose how to make operable vertical DMOSFETs at all possible dimensions down to and including zero JFET width." *Id.* at 16 n.8.

With respect to the upper boundary, Defendants contend that the phrase "less than about" does not express precise boundaries on the scope of the term. *Id.* at 17. Defendants contend that when "'about' is used as part of a numeric range, '[its] meaning depends on the technological facts of the particular case." *Id.* (quoting *Cohesive Techs., Inc. v. Waters Corp.*, 543 F.3d 1351, 1368 (Fed. Cir. 2008)). Defendants contend that, in this case, neither the specification or the knowledge of a POSITA provides a basis determining of the scope of the claim term with reasonable certainty

for at least the following reasons. *Id.* at 17–18. First, Defendants contend that the specification does not describe purpose of what "less than about three micrometers" is supposed to achieve for the claimed MOSFET device. *Id.* at 18. Defendants contend that the specification "concedes that selection of various design parameters (including JFET width) depends on 'desired characteristics' of the MOSFET device, but fails to provide any characteristics motivating the selection or required precision of the 3-micrometer JFET measurement." *Id.*

Second, Defendants contend that "the technical subject matter and knowledge of a POSITA provide no more certainty regarding the purpose for the 'less than about three micrometers' JFET-width limitation or the acceptable boundaries of that range." *Id.* at 19. Rather, Defendants contend that different selections of MOSFET parameters create design trade-offs. *Id.* (quoting IEEE paper by a co-inventor). Defendants contend that the specification and claim do not describe any combination of design parameters that would "influence or inform what is within the claimed range for the JFET width, therefore, the choice is up to the "subjective personal choice" of the designer. *Id.* at 19–20.

In its response, Plaintiff first contends that Defendants essentially conceded that a POSITA would understand the meaning of this term as it said that the PTAB did not need to construe any terms during an IPR and was able to determine if prior art fell within the scope of this term. Response at 10–11.

Second, Plaintiff second contends that terms of approximation like "about" or "at least about" are common in patent law and the Federal Circuit has confirmed that they are not indefinite. *Id.* at 11 (citing *Ecolab, Inc. v. Envirochem, Inc.*, 264 F.3d 1358, 1367 (Fed. Cir. 2001)). Plaintiff contends that the Federal Circuit has construed "about" to mean "approximately." *Id.*

Plaintiff contends that "[b]ecause it is rarely feasible to attach a precise limitation to "about," this qualifying language generally must be understood in light of the technology embodied in the invention." *Id.* (quoting *Modine Mfg. Co. v. United States Int'l Trade Comm.*, 75 F.3d 1545, 1554 (Fed. Cir. 1996), abrogated in nonrelevant part by *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 234 F.3d 558 (Fed. Cir. 2000) (en banc)) (internal quotation marks omitted). Plaintiff contends that, in this case, "about" means ±10% due to manufacturer tolerances. *Id.* at 12.

Third, Plaintiff contends that the specification informs a POSITA about the scope of this term with reasonable certainty. *Id*. In particular, Plaintiff contends that the specification describes that JFETs may have a width of "less than about 3 micrometers" and that the width may be "about one micrometer." *Id.* (citing 1:65-67, 2:47-49; 3:26; 6:24-27). Plaintiff contends that a POSITA would understand that the purpose of reducing JFET width is to increase cell density and reduce on-state resistance. *Id.* at 12–13 (citing 1:27–33, 6:21–24).

With respect to the lower bound, Plaintiff contends that a POSITA would understand that this term does not go down to 0 μm and that Defendants concede that a 0 μm device would not be a MOSFET. *Id.* at 13.

In their reply, Defendants first contend that Plaintiff's expert opinion with respect to the upper boundary is conclusory and unsupported, and thus should be disregarded. Reply at 6. In particular, Defendants contend that the Plaintiff's "only support for the upper limit of the range is a conclusory statement by its expert, Dr. Bhat, that a POSITA would interpret 'about' as implying 3.0 JFET width with a 10% variation (so 'about 3' means 3.3)." *Id.* But Defendants contend that Plaintiff's argument is "problematic" for several reasons. First, Defendants contend that Plaintiff's expert's opinion is conclusory and unsupported. *Id.* Second, Defendants contend that nothing in

the patent suggests that "about" is directed towards manufacturing variations. *Id.* at 7. Rather, Defendants assert that because the patent does not describe any performance goal, there is no indication as to how much the parameter can vary above 3 μm. *Id.*

Defendants contends that to the extent Plaintiff's expert was suggesting that as close to 3.0 μm is "optimal," Plaintiff's expert is mistaken because: 1) The range of values for the claim is 0 to 3 μm, which means it covers a wide range of non-optimal values, 2) While 3 μm was optimal for Ryu prior art, that was for a specific combination of voltages, thicknesses, and concentrations, which Claim 9 does not specify. *Id.* at 7. Defendants contend that Ryu explains that when 5 μm may more optimal once manufacturing variations are considered. *Id.*

Defendants contend that Plaintiff have not shown that a POSITA could determine the lower boundary with reasonable certainty. *Id.* Defendants contend that Plaintiff does not provide any evidence that would allow a POSITA to determine what the lower boundary of the claimed range is. *Id.* at 8. Defendants contend that the evidence Plaintiff cites shows that widths less than 1 μm have a "severely negative" effect on performance. *Id.* Defendants contend that Plaintiff "proposes a moving target: the lower limit is as small as someone is able to make a device until someone else is able to make one even smaller." *Id.*

Defendants contend that their IPR petitions do not undermine their positions in district court. *Id.* In particular, Defendants contend that claim construction is only necessary in order to resolve the IPR. *Id.* at 8–9. Defendants contend that they "merely stated no constructions are required because the prior art invalidates regardless of the constructions: '[G]iven the close correlation between the asserted prior art and the challenged claims . . . any reasonable interpretation . . . reads on the prior art.'" *Id.* at 9 (quoting IPR petition).

Defendants also contend that its indefiniteness argument is like an "in the alternative" argument. *Id.* Defendants contend that one difference between the IPR proceeding and the district court case is that "the precise bounds of the term were irrelevant for the IPR because [Defendants] presented prior art clearly covering any potential interpretation, whereas the issue before this Court is whether the upper and lower boundaries of the claim are sufficiently clear." *Id.* at 9–10.

In its sur-reply, Plaintiff contends that Defendants have not provided clear-and-convincing evidence. Sur-Reply at 5. Plaintiff first contends that Defendants' expert is not a POSITA and thus Defendants' arguments are "devoid of support." *Id.*

Plaintiff next contends that Defendants do not "challenge the fact that terms of approximation like 'about' or 'at least about' are ubiquitous in patent claims, well-understood, and do not render patent claims indefinite. Thus, 'less than about' here means 'less than approximately.'" *Id.* at 6.

Plaintiff next contends that Defendants' boundary arguments "lack merit." *Id.* With respect to Defendants' upper boundary arguments, Plaintiff contends that the width is optimized to reduce the on-resistance and the electric field. *Id.* Other design objectives include ensuring good forward current conduction and withstanding reverse blocking voltage. *Id.* With respect to Defendants' lower boundary arguments, Plaintiff contends that specification provides an example where the width is less than 3 μm (1 μm). *Id.* Plaintiff contends that a POSITA would know the minimum cannot be 0 μm or something infinitesimally small. *Id.*

With respect to the ±10% tolerance argument, Plaintiff contends that this variation is well-understood in the field. *Id.* at 6–7 (citing textbook).

The Court's Analysis:

After reviewing the parties' arguments and considering the applicable law, the Court agrees with Plaintiff that the term is not indefinite and should be construed according to its plain-and-ordinary meaning for the reasons that follow. ***First***, with respect to the lower boundary, the claim term only requires that the width of the JFET region needs to be less than 3 μm. '633 Patent, Cl. 9, Lim. [i]. It does not, however, specify a minimum. Therefore, a POSITA would understand that a JFET width less than 3 μm meets the claim limitation. ***Second***, a POSITA would know, with at least reasonable certainty, that the minimum lower bound is the minimum feature size (along with some very slight manufacturing variation), *i.e.*, the minimum size that can be manufactured. ***Third***, even if the JFET width was 0 μm, then it would not meet the other claim elements, *e.g.*, the semiconductor device would not be a field-effect transistor. Therefore, with respect to the lower boundary, the Court concludes that the claim term is not indefinite as a POSITA would understand with reasonable certainty the scope of the claim term.

With respect to the upper boundary, the Court concludes that the evidence that Defendants provides is not clear-and-convincing for the reasons that follow. ***First***, terms of approximation like "about" or "at least about" are common in patent law and the Federal Circuit has confirmed that they are not indefinite. *Merck & Co. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1369 (Fed. Cir. 2005). Defendants do not appear to dispute this. ***Second***, a POSITA would understand that semiconductor fabrication is not an absolutely precise process, but like other manufacturing processes, there are small variations. *See, e.g.*, Response, Bhat Declaration at ¶ 12. As such, the Court finds that a POSITA would understand that "about" is not indefinite, but rather, at minimum, was intended to account for well-known fabrication variation. ***Third***, the specification provides design guidance and objectives including optimizing the width to reduce the on-resistance and the

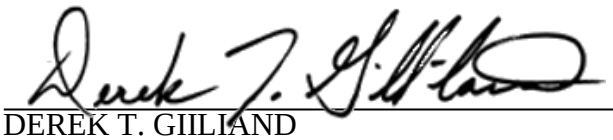
electric field, and ensuring good forward current conduction and withstanding reverse blocking voltage. *See, e.g.*, '633 Patent at 1:18–36.

Therefore, for the reasons described above, the Court concludes that Defendants have not met their clear-and-convincing burden to show that a POSITA would not understand, with reasonable certainty, that this term is indefinite. As such, because the "heavy presumption" is that terms should have their plain-and-ordinary meaning, the Court's final construction for "less than about three micrometers" is not indefinite, plain-and-ordinary meaning.

IV. CONCLUSION

In conclusion, for the reasons described herein, the Court adopts the below constructions as its final constructions.

SIGNED this 14th day of December, 2022.



DEREK T. GIILIAND
UNITED STATES MAGISTRATE JUDGE

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Final Construction
#1: "a second, thicker oxide layer" / "a gate oxide layer" U.S. Patent No. 8,035,112, Cls. 1, 6	"layer of oxide that is on the tops and sides of each gate and that is thicker than the layer of oxide below each gate"	"an oxidation layer formed, created, or grown by reacting the gate, thicker than the first oxide layer"	Plain-and-ordinary meaning
#2: "double-implanted metal-oxide semiconductor field effect transistor" U.S. Patent No. 7,498,633, Cl. 9	The preamble is not limiting. In the alternative only, "double-implanted" is not limiting.	The preamble **is** limiting.	The preamble is limiting.
#3: "less than about three micrometers" U.S. Patent No. 7,498,633, Cl. 9	Plain and ordinary meaning, no construction necessary.	Indefinite	Not indefinite. Plain-and-ordinary meaning.